What is claimed is:

1. A control method of a semiconductor memory device comprising the steps of:

first operation step executed in accordance with first operation sequence;

second operation step executed in accordance with second operation sequence separately from the first operation step; and

control step for delaying predetermined state transition to be executed in the second operation step following an instruction of the second operation sequence in accordance with predetermined first operation state in the first operation sequence.

2. A control method of a semiconductor memory device according to claim 1, wherein the predetermined state transition delayed in the control step is at least one of following operation states, namely, start of the second operation step, end of the second operation step, and state change in the second operation step.

3. A control method of a semiconductor memory device according to claim 1, wherein the predetermined first operation state is an operation state due to a small amplitude signal, and the predetermined state transition is either voltage transition or current transition that is a noise source against an operation state caused by the small amplitude signal.

4. A control method of a semiconductor memory device according to claim 1, wherein the control step includes

response delay step for delaying a response to an instruction of the predetermined state transition in the second operation sequence based on the predetermined first operation state.

5. A control method of a semiconductor memory device according to claim 4, wherein the second operation step includes at least either one of voltage generate step or current generate step, and due to the response delay step, there is delayed state change of voltage or current such as change from non-output state to output state or change from output state to non-output state in the voltage generate step or the current generate step, respectively.

6. A control method of a semiconductor memory device according to claim 4, wherein the second operation step includes at least either one of voltage generate step or current generate step, and due to the response delay step, there is delayed starting or stopping generation of voltage or current in the voltage generate step or the current generate step, respectively.

7. A control method of a semiconductor memory device according to claim 4, wherein the second operation step include path form step, and due to the response delay step, there is delayed state change of a signal path establishment such as change from not-established to established state or change from established to not-established state in the path form step.

8. A control method of a semiconductor memory device according to claim 1, wherein the second operation step

includes state transition instruct step for giving an instruction of state transition for each predetermined time in accordance with the second operation sequence, and timer step for supplying timer information to the state transition instruct step, and the control step includes timer delay step for delaying supply timing of the timer information based on the predetermined first operation state.

9. A control method of a semiconductor memory device according to claim 8, wherein the timer step includes basic timer step for supplying the timer information per unit of basic time, and timer of the basic time in the basic timer step is stopped or delayed due to the time delay step.

10. A control method of a semiconductor memory device according to claim 9, wherein stop of the timer is conducted per unit of the basic time.

11. A control method of a semiconductor memory device according to claim 9, wherein delay of the timer is conducted by time responsive to the predetermined first operation state.

12. A control method of a semiconductor memory device according to claim 1, wherein the second operation step includes state transition instruct step for giving an instruction of state transition for each predetermined time in accordance with the second operation sequence, and the control step includes delay add step for delaying the instruction of the predetermined state transition based on the predetermined first operation state.

13. A control method of a semiconductor memory device according to claim 1, wherein the second operation step includes state transition instruct step for giving an instruction of state transition for each predetermined time in accordance with the second operation sequence, and the control step includes setting time adjust step for expanding the predetermined time in the state transition instruct step based on the predetermined first operation state.

14. A control method of a semiconductor memory device according to claim 1, wherein the semiconductor memory device includes non-volatile memory cells electrically rewritable, as memory cells.

15. A control method of a semiconductor memory device according to claim 14, wherein the first operation step is data readout operation step, and the second operation step is data write operation step.

16. A control method of a semiconductor memory device according to claim 15, wherein the data write operation step is data program step or data erase step.

17. A semiconductor memory device comprising:

a first circuit that outputs at least one first signal for first operation in accordance with first operation sequence; and

a second circuit that outputs at least one second signal for second operation executed separately from the fist

operation in accordance with second operation sequence,

wherein the second circuit is controlled by at least one predetermined first signal out of the at least one first signal, and an output of at least one predetermined second signal out of the at least one second signal is delayed.

18. A semiconductor memory device according to claim 17, wherein the predetermined second signal is a signal outputted with at least one of following timings, namely, start of the second operation, end of the second operation, and operation change due to the second operation sequence.

19. A semiconductor memory device according to claim 17, wherein the predetermined first signal is a signal of small amplitude signal operation in the first operation, and the predetermined second signal is a signal accompanying either voltage transition or current transition that is a noise source against the small amplitude signal operation.

20. A semiconductor memory device according to claim 17, wherein the second circuit includes a sequence controller section for controlling the second operation sequence, a signal output section for outputting the at least one second signal, in accordance with at least one control signal from the sequence controller section, and a response delay section for delaying output response of the at least one predetermined second signal with regard to at least one predetermined control signal among the control signals in the signal output section in accordance with the at least one predetermined first signal.

21. A semiconductor memory device according to claim 20, wherein the signal output section includes a voltage generator circuit or a current generator circuit, and due to the response delay section, there is delayed state change of voltage or current such as change from non-output state to output state or change from output state to non-output state.

22. A semiconductor memory device according to claim 20, wherein the signal output section includes a voltage generator circuit or a current generator circuit, and due to the response delay section, there is delayed starting or stopping circuit operation of the voltage generator circuit or the current generator circuit.

23. A semiconductor memory device according to claim 20, wherein the signal output section includes a switch circuit, and due to the response delay section, there is delayed open-close change timing of the switch circuit.

24. A semiconductor memory device according to claim 17, wherein the second circuit includes a sequence controller section for controlling the second operation sequence, a timer section for supplying the sequence controller section with timer information, and a timer delay section for delaying a timer operation in the timer section, in accordance with the at least one predetermined first signal.

25. A semiconductor memory device according to claim 24, wherein the timer section includes an oscillator section for outputting an oscillation signal of predetermined cycle, and

due to the timer delay section, there is executed stopping of an oscillation operation or cycle expanding of the oscillation signal.

26. A semiconductor memory device according to claim 25, wherein stopping of the oscillation operation is inhibition of signal transition in the oscillation signal.

27. A semiconductor memory device according to claim 25, wherein cycle expanding of the oscillation signal is time expanding responsive to activation time of the at least one predetermined first signal.

28. A semiconductor memory device according to claim 17, wherein the second circuit includes a sequence controller section for controlling the second operation sequence, and a delay adder section for delaying at least one predetermined control signal outputted from the sequence controller section, in accordance with the at least one predetermined first signal.

29. A semiconductor memory device according to claim 17, wherein the second circuit includes a sequence controller section for controlling the second operation sequence, and a setting time adjustor section for expanding setting time of predetermined operation sequence in the second operation sequence, in accordance with the at least one predetermined first signal.

30. A semiconductor memory device according to claim 17 further comprising electronically rewritable non-volatile

memory cells as memory cells.

31. A semiconductor memory device according to claim 30, wherein the first operation is data readout operation, and the second operation is data write operation.

32. A semiconductor memory device according to claim 31, wherein the data write operation is data program operation or data erase operation.